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Domain decomposition techniques for microelectronic modeling *

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Abstract

This paper is meant to be the continuation of the previous work [1] where a coupled ODE/PDE method for the simulation of semiconductor devices was introduced. From a strictly mathematical viewpoint, analytical results on coupled PDE/ODE systems (as arising in integrated circuit simulation) can be found in [2]. In particular, in the present paper, we numerically investigate an algorithm of Domain Decomposition type for the simulation of circuits containing distributed devices (§ 1) as well as semiconductors in which some part is modeled with lumped parameters (§ 2). It is worth noticing the original employment of the Domain Decomposition technique within the confines of a “heterogeneous” PDE/ODE coupling, versus its typical use in a “homogeneous” full-PDE context. The results presented here have been studied in the seminal work [3], while a more thorough analysis is ongoing [4].

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1 Extra-device approach

The approach that we present here is devoted to circuit analysis. Suppose we have to deal with a complex circuit network where, however, only few devices are critical with respect to the behavior of the network. On the one hand, the use of a complex PDE model to describe the whole network may be unnecessary and, even though very accurate, it would also require a lot of resources, thus undermining the overall efficiency. On the other hand, using some “black box” method to model the critical devices would possibly be quite inaccurate. What we propose here is to use the PDE model only where strictly needed, keeping the lumped circuit model for the other parts. In the literature, this kind of heterogeneity is usually addressed as mixed-mode device simulation and a Newton-like numerical procedure is implemented in the simulator MINIMOS-NT [5]. Recently the full Newton method has also been applied to the simulation of a coupled semiconductor-circuit model including thermal effects [6]. Our approach is instead based on Domain Decomposition techniques that suitably allows for the coupling of distributed devices, modeled by PDE’s, with external circuits described by ODE’s. With this aim we have employed a suitable extension of the Dirichlet/Neumann algorithm [7] to enforce the continuity of both currents and node potentials at the device-circuit interface.

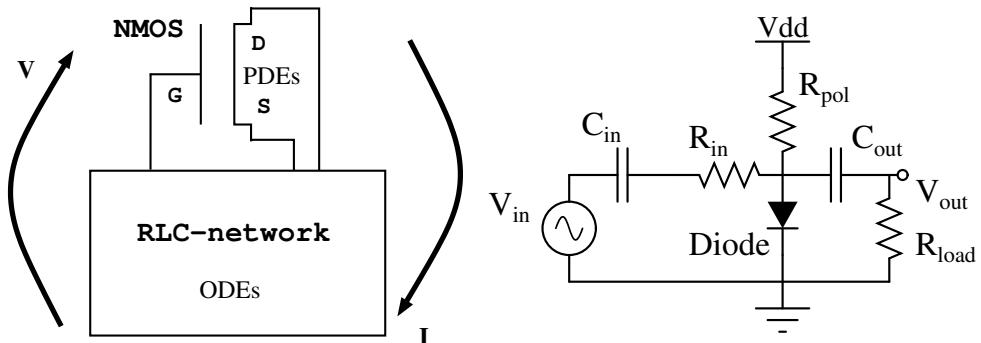


Figure 1: Example of the Domain Decomposition approach for network analysis (left) and scheme for the attenuator of the model problem (right)

For simplicity, suppose that there is only one device that requires a PDE description like, for example, a *pn* junction diode. We can consider the circuit viewed from the diode terminals as a generic bipole: thus the circuit is divided in two separate subdomains, i.e., the PDE-diode and the ODE-bipole. To apply the Dirichlet/Neumann algorithm it is necessary to figure out how to treat the boundary conditions (b.c.). We have chosen to use Neumann b.c. (i.e., current-operated) for the ODE-circuit and Dirichlet b.c. (voltage-operated) for the PDE-diode. To fix some notation, suppose that the distributed and the lumped models are described by the two problems

$$\frac{\partial u}{\partial t} + \mathcal{D}(u, V) = 0 \quad \text{in } \Omega \times (0, T], \quad \text{and} \quad \frac{dw}{dt} + \mathcal{L}(w, I) = 0 \quad \text{in } (0, T], \quad (1)$$

respectively, where $u = u(x, t)$ represents the internal (state) variable of the PDE part, with $x \in \Omega$ and $t \in (0, T]$, $w = w(t)$ those of the ODE, while $V = V(t), I = I(t)$ are the vectors of the potentials and of the currents, respectively,

Table 1: Numerical data used for the extra-device test case

Diode	P Zone	N Zone
Doping (Uniform)	$N_A = 10^{17} \text{ cm}^{-3}$	$N_D = 10^{17} \text{ cm}^{-3}$
Length	$5\mu\text{m}$	$5\mu\text{m}$
Minority carrier lifetime	10 ns	10 ns
Simulation time		$1\mu\text{s}$
Time step		5 ns
Circuit		
$R_{\text{in}} = 100 \text{ k}\Omega$	$R_{\text{pol}} = 100 \text{ k}\Omega$	$R_{\text{load}} = 1 \text{ k}\Omega$
$C_{\text{in}} = 10 \text{ nF}$	$C_{\text{out}} = 10 \text{ nF}$	
$V_{\text{DD}} = 5 \text{ V}$	$V_{\text{in}} = \sin(2\pi ft) \text{ mV}$	$f = 1 \text{ MHz}$

at the boundary of the device occupying the domain Ω . The quantities \mathcal{D}, \mathcal{L} are suitable differential operators and proper boundary and initial conditions are understood. Let us first introduce a partition $\{t_n\}$ of $[0, T]$ into N subintervals such that $0 = t_0 < t_1 < \dots < t_{N-1} < t_N = T$. We want to advance the solutions $u(x, t), w(t)$ from $t = t_n$ until $t = t_{n+1}$, for $n = 0, 1, \dots, N - 1$. The Dirichlet/Neumann algorithm can be thought of as a fixed point iteration for the potentials $V(\cdot)|_{(t_n, t_{n+1})}$. For this purpose, set the iteration counter $j \leftarrow 0$. Then given some initial guess $V^{(j)}$, the algorithm comprises the following steps:

1. Solve $\frac{\partial u}{\partial t}^{(j+1)} + \mathcal{D}(u^{(j+1)}, V^{(j)}) = 0$ in $\Omega \times (t_n, t_{n+1}]$ for $u^{(j+1)}(x, t)$;
2. Compute $I^{(j+1)} = \mathcal{I}(u^{(j+1)}, V^{(j)})$;
3. Solve $\frac{dw}{dt}^{(j+1)} + \mathcal{L}(w^{(j+1)}, I^{(j+1)}) = 0$ in $(t_n, t_{n+1}]$ for $w^{(j+1)}(t)$;
4. Compute $V^{(j+1)} = \theta \mathcal{V}(w^{(j+1)}, I^{(j+1)}) + (1 - \theta) V^{(j)}$;
5. Check for convergence: if $\|V^{(j+1)} - V^{(j)}\|_{(t_n, t_{n+1})} < \varepsilon$ then finish, else $j \leftarrow j + 1$ and go to 1.

Note that the functions $I = \mathcal{I}(u, V), V = \mathcal{V}(w, I)$ return the output current of the device and the potentials at the circuit terminals, respectively, while $0 < \theta < 1$ is a suitable relaxation parameter, and ε a given tolerance. In practice, the fixed point mapping is understood with respect to the final value $V(t_{n+1})$ only, and spatial/temporal discretization schemes have to be employed as well. This algorithm admits also a very interesting circuit interpretation, see Fig. 1 (left). As we can identify Neumann b.c. with the currents at the diode terminals, and Dirichlet b.c. with the values of the corresponding potentials, we have to deal at each time step with a voltage-operated PDE device and with a current-operated ODE circuit. We point out that this procedure is implementable without any knowledge about the internal codes of both the PDE and the ODE solvers. Actually, one can use these particular solvers as building-blocks for implementing the Domain Decomposition algorithm.

We carry out a sensitivity analysis with respect to the relaxation parameter of the Dirichlet/Neumann algorithm for the transient simulation of a small signal circuit, i.e., an attenuator (Fig. 1, right). The diode is treated as a 1D device

and is described by the Drift-Diffusion (DD) transport model [8]. The data used in the simulation are gathered in Tab. 1. The circuit is solved via the Tableau analysis [9]. The sensitivity for both Dirichlet (top) and Neumann (bottom) b.c. is shown in Fig. 2, where the number of iterations vs time and relaxation parameter are displayed. Notice that under-relaxation is needed for convergence with an optimal parameter of about 0.15 in both cases.

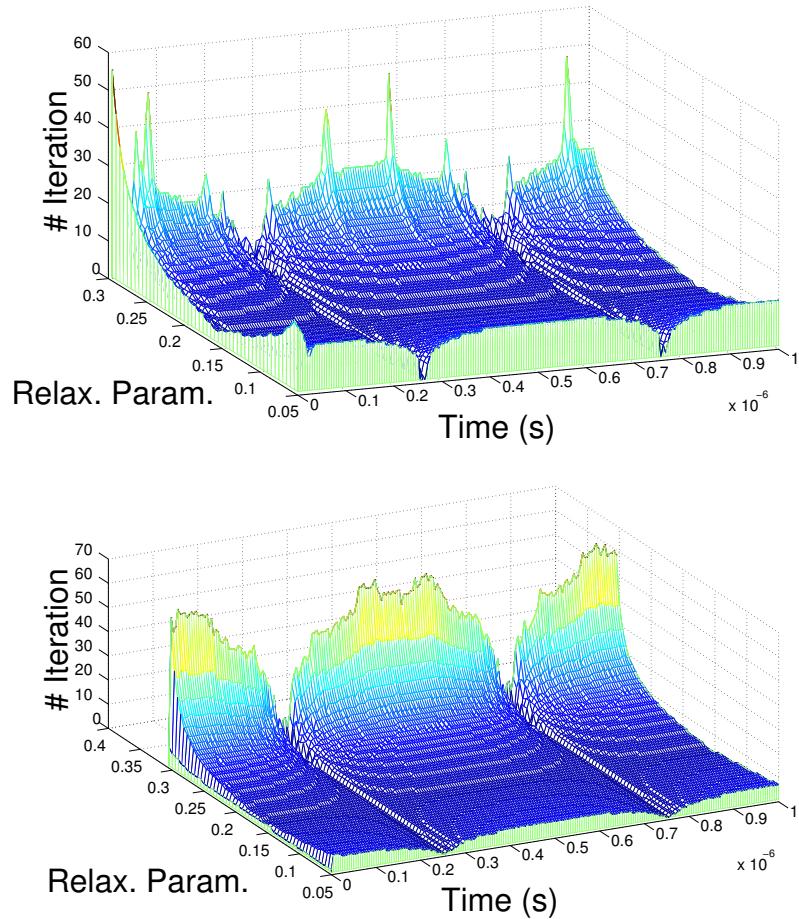


Figure 2: Sensitivity for Dirichlet (top) and Neumann b.c. (bottom)

2 Intra-device approach

The second approach we present is focused on the simulation of a single distributed device. In this case we treat with a PDE model a particular region of interest of the device at hand, and with an ODE model the other parts. As in the extra-device case, the terminal current and voltage continuity is enforced via the Dirichlet/Neumann approach. In Fig. 3 (left) we see a possible application of this procedure to a MOSFET where only the channel (green box) is modeled with PDE's. For the derivation of a suitable ODE model we have used a technique proposed in [10, 1] that allows for the extraction of a compact *physics-based* circuit model from dc device simulations. We have also improved the model, deriving the constitutive relations for the currents from a linearization of the very

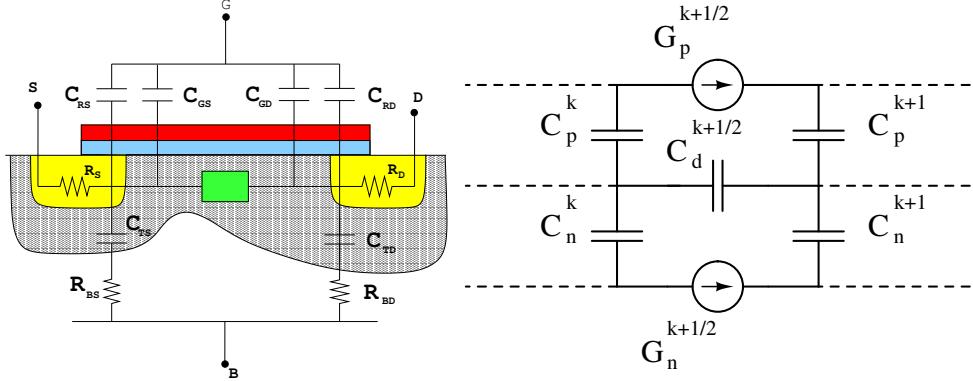


Figure 3: Example of ODE/PDE coupling for a single device (left) and basic building-block for the circuit extraction technique (right)

well-known Scharfetter-Gummel formulas [11]. This has the advantage of being mathematically consistent with the PDE model, where the current continuity equations are also discretized via the Scharfetter-Gummel formulas, and eliminates the degree of freedom in the choice of the conductances that characterizes the approach in [10]. In particular, the expressions of the conductances for the electrons read:

$$G_{mn}^{k+1/2} = -\frac{q\mu_n}{h} \left[\dot{B}(\Delta_k \psi) n_{k+1} + \dot{B}(-\Delta_k \psi) n_k \right],$$

$$G_{rn}^{k+1/2} = \frac{q\mu_n}{h} B(\Delta_k \psi) n_{k+1}, \quad G_{fn}^{k+1/2} = -\frac{q\mu_n}{h} B(-\Delta_k \psi) n_k,$$

where q is the absolute value of the electron charge, μ_n the electron mobility, h the length of a typical grid element, n_k, ψ_k the electron concentration and electric potential at the k -th grid point, $\Delta_k \psi = \frac{\psi^{k+1} - \psi^k}{V_{th}}$, $B(\cdot), \dot{B}(\cdot)$ the Bernoulli function and its derivative, while V_{th} is the thermal voltage.

The algorithm that we propose is in some way similar to the one adopted in the extra-device case, except that we have to guarantee that the ODE system be consistent with the PDE model. This is why we have used a physics based circuit extraction that calibrates the lumped model from dc device simulations only. Basically, this procedure allows us to describe a semiconductor region of finite size with the basic circuit block shown in Fig. 3 (right).

We have tested our algorithm on a model problem, i.e., a voltage-operated 1D diode. We use the lumped model only in the quasi-neutral zones, while the PDE model (based on the DD equations) is employed for the depletion region. This choice is motivated by the consideration that this region is where most of the physically relevant processes take place, so that it represents the part of the device needing a more accurate description.

We carry out a sensitivity analysis with respect to the relaxation parameter for a transient simulation. The Gummel map [12] is employed for the solution of the DD equations. The data used in the simulation are collected in Tab. 2. The lumped circuits are solved with the MNA analysis [9, 13]. The sensitivity results are displayed in Fig. 4, through the number of iterations vs time and relaxation parameter, and where the order of the circuits refers to the number of blocks used for modelling each quasi neutral zone. The relaxation refers only to the

Table 2: Numerical data used for the intra-device test case

Diode	P Zone	N Zone
Doping	$N_A = 10^{16} \text{ cm}^{-3}$	$N_D = 10^{16} \text{ cm}^{-3}$
Mobility	$1000 \text{ cm}^2/(\text{V s})$	$1000 \text{ cm}^2/(\text{V s})$
Length	$5\mu\text{m}$	$5\mu\text{m}$
Polarization	0.6 V	No Generation/Recombination
ac signal	$\sin(2\pi ft) \text{ mV}$	$f = 100 \text{ kHz}$

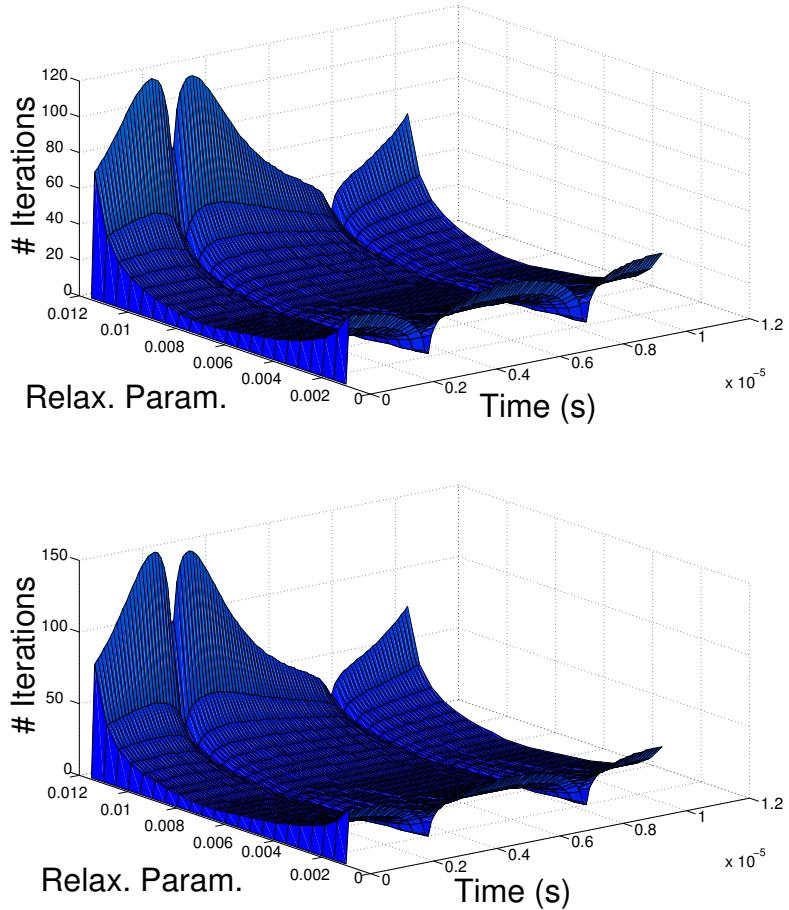


Figure 4: Sensitivity analysis for the coupled model with fifth- (top) and tenth-order circuits (bottom)

Neumann boundary conditions. As in the extra-device case, under-relaxation is required for convergence and the optimal parameter is about 0.007.

3 Conclusions

We have extended a Dirichlet-Neumann method to the ODE/PDE framework for simulating extra-device as well as intra-device structures. The numerical investigations show that under-relaxation is required for achieving convergence under

general conditions. Moreover, also a time adaptive procedure would be welcome for a better efficiency. So far only simple devices and (linear) circuits have been tested. We plan to extend the numerical technique to more complex circuits and to multidimensional devices, and to carry out a theoretical assessment of the convergence properties of the whole algorithm.

References

- [1] Alì, G., Micheletti, S.: Domain Decomposition techniques and coupled PDE/ODE simulation of semiconductor devices. In Anile, A., Alì, G., Mascali, G., eds.: Scientific Computing in Electrical Engineering. Volume 9 of Mathematics in Industry., Berlin, Springer (2006) 407–411
- [2] Alì, G., Bartel, A., Günther, M., Tischendorf, C.: Elliptic partial differential algebraic multiphysics models in electrical network design. *Math. Models Methods Appl. Sci.* **13** (2003) 1261–1278
- [3] Culpo, M.: Accoppiamento Eterogeneo ODE/PDE per il Trasporto di Carica nei Semiconduttori. Master thesis, Politecnico di Milano (2006)
- [4] Alì, G., Culpo, M., Micheletti, S.: In preparation. (2006)
- [5] Grasser, T.: Mixed-Mode Device Simulation. Dissertation, Technische Universität Wien (1999)
- [6] Brunk, M., Jüngel, A.: Numerical coupling of electric circuit equations and energy-transport models for semiconductors. Submitted (2007)
- [7] Quarteroni, A., Valli, A.: Domain Decomposition Methods for Partial Differential Equations. The Clarendon Press, Oxford University Press, New York (1999)
- [8] Selberherr, S.: Analysis and Simulation of Semiconductor Devices. Springer-Verlag, Wien, New York (1984)
- [9] Chua, L., Desoer, C., Kuh, E.: Linear and Nonlinear Circuits. McGraw-Hill (1987)
- [10] Pacelli, A., Mastrapasqua, M., Luryi, S.: Generation of equivalent circuits from physics based device simulation. *IEEE Trans. Circuits Syst.* **19** (2000) 1241–1250
- [11] Scharfetter, D., Gummel, H.: Large signal analysis of a silicon read diode oscillator. *IEEE Trans. Electron Devices* **16** (1969) 64–77
- [12] Gummel, H.: A self-consistent iterative scheme for one dimensional steady-state transistor calculations. *IEEE Trans. Electron Devices* **11** (1964) 455–465
- [13] Ho, C., Ruehli, A., Brennan, P.: The modified nodal approach to network analysis. *IEEE Trans. Circuits Syst.* **22** (1975) 504–509